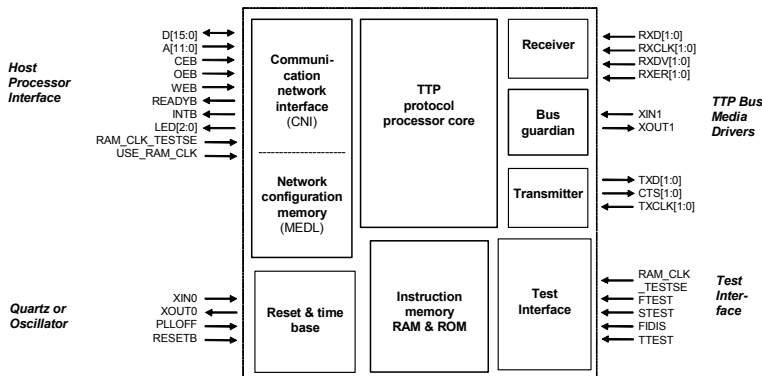


## Fast TTP Communication Controller – C2NF



## OVERVIEW

This TTP controller is a high-speed version of the C2 controller series designed by TTTech. The RISC core is optimized for internal processing speed of 40 MHz and has an inter frame gap (IFG) reduced to 22 µs resulting in a higher data throughput. The C2NF can be configured to suite a wide range of user requirements and to work with Intel-Type MCU bus interfaces with data widths of 16 bits. It permits easy integration into custom System-on-Chip designs. This version of TTP controller supports communication speeds of 5 Mbit/s with MFM or Manchester coding on two channels, as well as a communication speed of 25 Mbit/s in synchronous mode (using a MII interface).

The C2NF RISC core design is compatible with TTP protocol specification V1.1 for fault-tolerant communication in distributed hard real-time systems. This fulfills stringent safety and redundancy requirements required for by-wire applications in automotive, aerospace, and industrial fields at a fraction of costs experienced in similar applications only few years ago.

The C2NF controller features 16k x 16 SRAM memory for message scheduling information (MEDL), CNI, status data, control data and message content. The RISC core uses separated 4k x 17 instruction RAM including parity check. Depending on the application, unused memory may be used by the external host. Application-specific data may be downloaded from the communication network or from the external host.

## DO-254/DO-178B Level A Certifiable

The C2NF chip IP is readily available for commercial applications. Examples of successful applications (based on the AS8202NF implementation by austriamicrosystems) include modular and distributed control systems in the Boeing 787 Dreamliner and the Airbus A380 as well as engine control in the Lockheed Martin F-16 and the Aermacchi M-346. The C2NF chip IP has been designed to meet aerospace requirements in compliance with DO-254 and DO-178B Level A and its AS8202NF implementation got certified within the Airbus A380 project.

## Product Features:

- 16 bit RISC core based
- Full protocol compatibility with TTP Specification V1.1
- Up to 5 Mbit/s asynchronous data transmission speed @ 40 MHz clock (MFM, Manchester coding)
- 25 Mbit/s synchronous data transmission speed @ 40 MHz clock
- 2 independent communication channels
- 16k x 16 internal RAM for scheduling information and CNI, accessible by a choice of Host CPU bus interfaces (Intel-Type)
- 4k x 17 instruction RAM with internal parity checking
- 128 x 16 DP synchronous RAM FIFO
- Fully scalable instruction code ROM (min. 2k x 16 up to 16k x 16) for int. protocol execution
- Versatile 16 bit bus interface
- 3 digital I/O ports
- Bus guardian on-chip

## Deliverables:

- Synthesizable netlist
- Implementation constraints
- Test benches
- Integration guide & data sheet
- Scheduling data (MEDL) specification

## **DESIGN FEATURES**

### **TTP Protocol Support**

The underlying communication principle is based on the time-triggered architecture and the TTP protocol – a mature and proven infrastructure for developing distributed hard real-time systems with stringent safety and redundancy requirements in aerospace, automotive and industrial applications. It also supports state of the art TTP X Frames for efficient communication.

### **Fault-Tolerant Communication**

The controller has a global time base with an accuracy better than 1µs and special on-chip services for detecting system failures at the protocol level. In order to tolerate different failure types, the TTP protocol supports various redundancy principles. Furthermore the C2NF calculates MEDL CRC with every access onto MEDL RAM providing even more security for the applications.

### **Composability**

This IP represents a fast-to-market technology for developing complex by-wire functional units that can be easily integrated with components from other suppliers. The 7<sup>th</sup> generation of tools for design of TTP-based systems is provided by TTTech Computertechnik AG ([www.tttech.com](http://www.tttech.com)).

### **Data Download**

The controller provides a data download service over the TTP network. This is very helpful for design updates i.e. the scheduling data can be easily updated in the final application (such as a car,

airplane or satellite). Obviously, with such approach the protocol updates and new features are just a download away.

### **Integrated Data Memory**

Due to the optimized scheduling information structure, available data memory (16k x 16) provides enough memory for different applications. The instruction RAM memory 4k x 17 (16 bit + parity bit) is reserved for TTP protocol firmware, providing flexibility of usage. Beyond that up to 16k x 16 ROM block makes stand-alone operation after power up possible. Free internal memory can be also used for other application-specific data required by the host controller. The memory is divided into pages and can be simultaneously accessed by the TTP controller and external host.

### **Integrated Bus Guardian**

The bus guardian is integrated on chip and is clocked by its own oscillator for safety reasons.

### **Digital I/O Pins**

Digital inputs/outputs can be configured for special application needs.

### **Programmable Bus Access Interface**

The controller supports 16 bit external bus access (Intel-Type). Advanced access modes such as read-ahead & posted write are supported for enhanced throughput, providing superior host communication performance

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