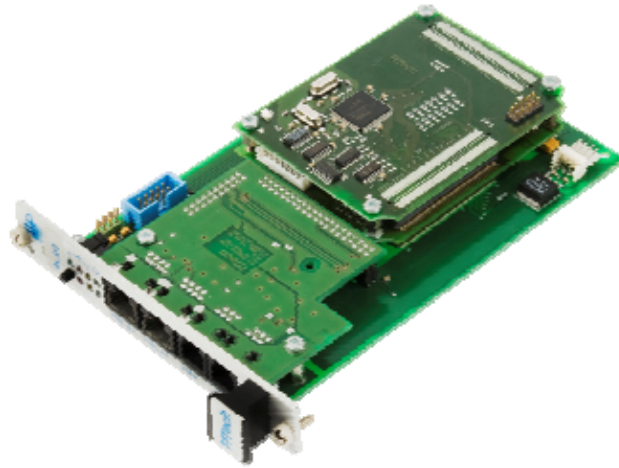


# TTP Powerlink

*The Modular TTP Development Board*



**TTP Powerlink is a high-performance, stacked-board expansion system solution for distributed hard real-time systems. It supports a broad range of interfaces and can be equipped with a Freescale MPC555 PowerPC®, a Freescale MPC5554 PowerPC®, a Freescale S12X microprocessor or an Infineon TriCore. Full embedded software and tool support is available.**

## Hardware Basics

TTP Powerlink has a rich set of integrated peripheral devices well suited for demanding prototyping applications. TTP Powerlink is equipped with an austriamicrosystems AS8202NF TTP communication controller. An integrated CAN controller provides features to design gateway units for coupling the CAN field bus with TTP.

External connectors for TTP and CAN are available on separate physical layer boards which are stacked onto the TTP Powerlink board. This allows a flexible choice of the physical layer for the MII and MFM/Manchester interfaces of the TTP controller.

The TTP Powerlink can be supplied with or without housing and power supply.

## KEY FEATURES/BENEFITS

- Full embedded software support
- Full tool support
- Multiple CPU options
- Exchangeable physical layer
- Exchangeable CPU
- Broad range of interfaces
- austriamicrosystems AS8202NF TTP communication controller
- Available with or without housing

## Software Support

TTP Powerlink is supported with a wide range of embedded software and tools.

It works perfectly with tools such as TTP Matlink. The code generated by the Real-Time Workshop® Embedded Coder via TTP Matlink supports rapid application development with automatic code generation.

A bootloader, an operating system, different communication layer options, and a powerful library for the MPC555 I/O are available for TTP Powerlink.

### Physical Specifications

- Single height standard Euro PCB
- Dimensions: 160 x 100 x 20, with housing and power supply 220 x 145 x 26 (in mm)
- Weight: 720 g; without housing 130 g
- Operating temperature: 0 °C to +70 °C, industrial grade (-40 °C to +85 °C) on request
- Storage temperature: -40 °C to +85 °C

### Power Requirements

- 5 V DC, +/- 5 % at 1A plus 12 V DC, +/- 5 % at 150 mA (without housing)
- Input voltage 9 to 60 V DC at max. 10 Watt and max. 1.2 A (with housing and power supply)

### Physical Layer Boards

There are 2 types of physical layer boards:

- MFM/Manchester on RS 485 physical layer (5 Mbit MFM/Manchester) for TTP
- MII: IEEE 802.3 100BASE-TX physical layer (25 Mbit MII) for TTP, requires 100Base-TX hub and star architecture

Both types support

- ISO 9141 physical layer suitable for LIN
- ISO 11898 physical layer for CAN (1 channel, Philips 82C250, RJ-11 connector)

### Additional Interfaces

- Serial communication interface (PCB-mounted connectors)
- User programmable LEDs on the front panel
- I/O reset button located on the front panel
- All port and timer pins of the CPU available on PCB-mounted connectors
- 32 analog inputs (PCB-mounted connectors) for Freescale MPC555 and MPC5554 PowerPC®
- On-line debug interface for Freescale MPC555 and MPC5554 PowerPC®

### Host CPUs

- Freescale MPC555 with floating point running at 40 MHz
  - 512 kB RAM (256 K x 16 bit) plus 10 Kbyte internal static RAM
  - 2 MB (1024 K x 16 bit) Flash plus 256 kB internal Flash memory
- Freescale MPC5554 based on the PLCB1 bus specification running at 132 MHz
  - 64 kB internal RAM
  - 1 MB external asynchronous SRAM
  - 2 MB external burstable Flash memory
- The following CPUs are available on request:
  - Freescale MC9S12XDP512 running at 40 MHz internal speed (20 MHz bus speed); 512 kB internal flash memory; 32 kB RAM; 4 kB EEPROM; 2 MB external Flash memory; 512 kB external RAM
  - Infineon TC1775 TriCore CPU running at 40 MHz; 512 kB external SRAM; 72 kB on Chip SRAM; 2 MB external burstable Flash memory

### Order Number

- H20.04.3: <sup>TTP</sup>Powerlink/MPC555 and MFM/Manchester physical layer
- H20.10.3: <sup>TTP</sup>Powerlink/MPC555 and MII physical layer
- H20.19.1: <sup>TTP</sup>Powerlink/MPC5554 and MFM/Manchester physical layer
- H20.21.1: <sup>TTP</sup>Powerlink/MPC5554 and MII physical layer

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